Introduction to CMOS RF Integrated Circuits Design

VI. Phase-Locked Loops
Outline

• Introduction
• Basic Feedback Loop Theory
• Circuit Implementation
What is a PLL?

A PLL is a negative feedback system where an oscillator-generated signal is phase and frequency locked to a reference signal.

Can be used as:
- Frequency Synthesis (e.g. generating a 1 GHz clock from a 100 MHz reference)
- Skew Cancellation (e.g. phase-aligning an internal clock to the IO clock) (May use a DLL instead)
- Extracting a clock from a random data stream (e.g. serial-link receiver)
Charge-Pump PLL Block Diagram

PFD → CP → VCO

Vctl

C1, C2

FbClk → DIV → Clk
Components in a Nutshell

- PFD: outputs digital pulse whose width is proportional to phase error
- CP: converts digital error pulse to analog error current
- LPF: integrates (and low-pass filters) error current to generate VCO control voltage
- VCO: low-swing oscillator with frequency proportional to control voltage
- DIV: divides VCO clock to generate FBCLK clock
• PLL is 2nd-order system similar to mass-spring-dashpot or RLC circuit.
• PLL may be stable or unstable depending on phase margin (or damping factor).
• Phase margin is determined from linear model of PLL in frequency-domain.
• Find phase margin/damping using MATLAB, loop equations, or simulations.
• Stability affects phase error, settling, jitter.
• PLL acts as a low-pass filter with respect to the reference signal.
• Low-frequency reference modulation (e.g. spread-spectrum clocking) is passed to the VCO signal.
• High-frequency reference jitter is rejected.
• “Bandwidth” is the frequency at which the PLL begins to lose lock with the reference (-3dB).
• PLL acts as a high-pass filter wrt VCO noise.
• Bandwidth affects phase error, settling, jitter.
PLL Linear Model

\[ H(s) = \frac{\theta_{out}(s)}{\theta_{ref}(s)} = \frac{K_{PD}K_{VCO}F(s)}{s + \frac{K_{PD}K_{VCO}F(s)}{N}} \]

\[ \frac{\theta_e(s)}{\theta_{ref}(s)} = \frac{s}{s + \frac{K_{PD}K_{VCO}F(s)}{N}} \]
PLL Linear Model

\[ F(s) = \frac{1}{(1 + sRC)} \]

\[ H(s) = \frac{\theta_{\text{out}}(s)}{\theta_{\text{ref}}(s)} = \frac{NK_{PD}K_{VCO}}{s^2NRC + sN + K_{PD}K_{VCO}} \]

\[ H(s) = \frac{N\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \]

\[ \omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{NRC}} \]

\[ \xi = \frac{1}{2}\sqrt{\frac{N}{K_{PD}K_{VCO}RC}} \]
PLL Linear Model

\[ F(s) = \frac{1 + \tau_2 s}{1 + \tau_1 s} \]
\[ \tau_1 = (R_1 + R_2)C \]
\[ \tau_2 = R_2 C \]

\[ H(s) = \frac{s \omega_n (2\xi - \frac{N^2 \omega_n}{K_{PD} K_{VCO}}) + N \omega_n^2}{s^2 + 2\xi \omega_n s + \omega_n^2} \]

\[ \omega_n = \sqrt{\frac{K_{PD} K_{VCO}}{N \tau_1}} \]
\[ \xi = \frac{1}{2} \sqrt{\frac{K_{PD} K_{VCO}}{N \tau_1}} \left( \frac{\tau_2}{K_{PD} K_{VCO}} + \frac{N}{K_{PD} K_{VCO}} \right) \]
What Determines Stability and Bandwidth?

• Damping Factor (measure of stability)
• Natural Frequency (measure of bandwidth)
• Damping and natural frequency can be set independently by LPF resistor
Noise Model
Noise Model---Transfer Functions

\[ H(s) = \frac{\theta_{\text{out}}(s)}{\theta_{\text{ref}}(s)} = \frac{NK_{PD}K_{VCO}F(s)}{Ns + K_{PD}K_{VCO}F(s)} \]

\[ \frac{\theta_{\text{out}}(s)}{\theta_{\text{vco}}(s)} = \frac{Ns}{Ns + K_{PD}K_{vco}F(s)} \]

\[ \frac{\theta_{\text{out}}(s)}{\theta_{\text{vco}}(s)} = \frac{Ns}{Ns + K_{pd}K_{lf}K_{vco}} = \frac{s}{s + \omega_c} \]

For \( F(s) = K_{lf} \)
Noise Model
Noise Model

![Graph showing phase noise versus frequency for different components like Frequency Divider, Reference, Total, PFD, VCO, and Reference. The Y-axis represents phase noise in dBc/Hz, and the X-axis represents frequency in Hz.]
PLL Circuits

- Phase-Frequency Detector
- Charge-Pump
- Low-Pass Filter
- Voltage-Controlled Oscillator
- Voltage Regulator
Edge-triggered - Input duty-cycle doesn’t matter
Pulse-widths proportional to phase error
PFD Logic States

3 and “1/2” Output states
States:

<table>
<thead>
<tr>
<th>UP</th>
<th>Down</th>
<th>Effect:</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>No Change</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Slow Down</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Speed Up</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Avoid Dead-Zone</td>
</tr>
</tbody>
</table>
Example: PFD

- Ref
- FbClk
- UP
- Down
- Vctl
“Dead-zone” occurs when the loop doesn’t respond to small phase errors - e.g. 10 pS phase error at PFD inputs:

- PFD cannot generate 10 pS wide UP and Down pulses
- Charge-pump switches cannot turn on and off in 10 pS
- Solution: delay reset to guarantee min. pulse width (typically > 150 pS)
Charge Pump

• Converts PFD phase error (digital) to charge (analog)
• Charge is proportional to PFD pulse widths
  \[ Q_{cp} = I_{up} * t_{UP} - I_{dn} * t_{Down} \]
• \( Q_{cp} \) is filtered/integrated in low-pass filter
Charge Pump

- **VD**
- **D**
- **RE**
- **F**
- **VD**
- **D**
- **F**
- **B**
- **D**
- **R**
- **K**
- **C**
- **K**

**UP**
- **I_{cp}**

**Reset**
- **S_{up}**
- **S_{dn}**

**Down**
- **I_{cp}**
Charge Pump Design Considerations

• Equal UP/DOWN currents over entire control voltage range - reduce phase error.
• Minimal coupling to control voltage during switching - reduce jitter.
• Insensitive to power-supply noise and process variations – loop stability.
• Easy-to-design, PVT-insensitive reference current.
• Programmable currents to maintain loop dynamics (vs. M, fref)?
• Typical: 1μA (mismatch) < Icp < 50 μA (ΔVctl)
• Static Phase Error: in lock, net \textit{UP} and \textit{DOWN} currents must integrate to zero
  • If \textit{UP} current is 2X larger, then \textit{DOWN} current source must be on 2X as long to compensate
  • Feedback clock must lead reference for \textit{DOWN} to be on longer
• \( \text{Terr} = \text{Tdn} - \text{Tup} = \text{Treset} \times (\text{Iup}/\text{Idn} - 1) \)
• Phase error can be extremely large at low VCO frequencies (esp. if self-biased) due to mismatch in current mirrors (low $V_{gs}-V_t$)

• Increase $V_{gs}$ or decrease $\Delta V_t$ (large $W*L$)

• Typical static phase error $< 100$ pS
• PFD-CP correct at rate of reference (e.g. 10nS).
• Most phase error correction occurs near reference rising edge and lasts < 200 pS, causing a control voltage ripple.
• This ripple affects the VCO cycles near the reference more than VCO cycles later in the ref cycle, causing VCO jitter.
• Typ. Jitter << 1% due to Up/Down Mismatches
• Avoid ripple by spreading correction over entire ref cycle. (Maneatis JSSC ’03)
Simple Charge Pump

- \( R(\text{switches}) \) varies with \( V_{\text{ctl}} \) due to body-effect
- Use CMOS pass-gate switches for less \( V_{\text{ctl}} \) sensitivity
- Long-channel current sources for matching and higher \( R_{\text{out}} \)
Add cap to VirtVctl for volt. stability

Amp keeps Vds of current sources constant (Young ’92)
Amp sinks “waste” current when UP, DOWN off

Vamp should track Icp
• Switches closer to power rails reduce noise and $V_{ctl}$ dependence $\rightarrow$ $I_{cp}$ not constant with up/down

$m1, m4, m5, m8, m9$: long $L$

$m1, m4, m5, m8, m9$: long $L$
Charge Pump: switches reversed with fast turn-off

m1, m4, m5, m8, m9: long L
m11, m12: faster turn-off

(Ingino ‘01)
Simple Charge-Pump Bias

- \( I_b \sim \frac{(V_{dd} - V_t)}{R} \)
- \( I_b \) dependent on PVT
- Prefer low-\( V_t \), moderate-to-long \( L \) for process insensitivity, large \( W/L \) for low gate-overdrive
- Pro: Simple, stable. Con: \( V_{dd} \) dependence
VDD-Independent Ibias

- \( Ib \sim \frac{1}{R2} \)
- Con: requires start-up circuit not shown
Bandgap-Based Ibias

• $I_b \sim \frac{V_{\text{ref}}}{R}$
• Con: feedback loop may oscillate
  - cap added to improve stability
• Pro: VDD-independent, mostly Temp independent

\[ V_{\text{ref}} \]
\[ + \]
\[ - \]
\[ V_{\text{fb}} \]
\[ \text{m1} \]
\[ \text{m2} \]
\[ I_b \]
Low-Pass Filter

- Integrates charge-pump current onto C1 cap to set average VCO frequency ("integral" path).
- Resistor provides instantaneous phase correction w/o affecting avg. freq. ("proportional" path).
- C2 cap smoothes large IR ripple on Vctl
- Typical value: 0.5k < R_{lpf} < 20k\Omega
Low-Pass Filter Smoothing Cap ($C_2$)

- “Smoothing” capacitor on control voltage filters CP ripple, but may make loop unstable
- Creates parasitic pole: $\omega_p = 1/(R \ C_2)$
- $C_2 < 1/10*C_1$ for stability
- $C_2 > 1/50*C_1$ for low jitter
- Smoothing cap reduces “IR”-induced VCO jitter to < 0.5% from 5-10%
- $\Delta f_{vco} = K_{vco}I_{cp}{T_{err}}/C_2$
- Larger $C_2/C_1$ increases phase error slightly
Low-Pass Filter Smoothing Cap ($C_2$)

![Graph showing Pct. Frequency Overshoot vs. LPF $C_2/C_1$](graph.png)

- **Phase Step = 180° (8 nS), $M=16$, $D=0.9$, $v_{ref}/v_{in}=70$**
- **During Initial Lock, $M=16$**
- **During Initial Lock, $M=8$, $D=1.2$, $v_{ref}/v_{in}=50$**

*Graph image showing the relationship between Pct. Frequency Overshoot and LPF $C_2/C_1$.*
Low-Pass Filter Capacitors

- Even thick gate oxide may still leak too much
- Large filter cap ($C_1$) typically ranges from 50pF to 400 pF
- $C_1$ cap BW may be as low as $\sim$10X PLL BW for nearly ideal behavior
- Min $C_2$ BW set by $T_{\text{ref}}$
- Cap BW $\sim 1/RC \sim 1/L^2$
- Gate cap not constant with $V_{gs}$
PLL Suppression of VCO Noise

• PLL acts like a high-pass filter in allowing VCO noise to reach PLL output
• Need noise-immune VCO to minimize jitter
  • Feedback loop cannot react quickly.
• Power-supply noise is largest source of VCO noise
VCO Design Concerns

• Large frequency range to cover PVT variation:
• Single-ended or differential?
• Vco gain ($f_{vco} = K_{vco} \cdot V_{ctl}$) affects loop stability
• More delay stages $\rightarrow$ easier to initiate oscillation
  • Gain(DC) > 2 for 3 stages
  • Gain(DC) > $\sqrt{2}$ for 4 stages
Voltage Regulator/Filter

• Used to filter power-supply noise
typically > 20 dB (10x) PSRR over entire
frequency range
desire 30+ dB

• Secondary purpose is to set precise voltage level
for PLL power supply
usually set by bandgap reference
Bandgap Reference w/Miller Cap

- Stability and PSRR may be poor w/o Miller cap
- Miller cap splits poles. Can also add R in series w/Cc for more stability (Razavi ’00)