Introduction to CMOS RF Integrated Circuits Design

V. Voltage Controlled Oscillators
Outline

◆ Phase Noise and Spurs
◆ Ring VCO
◆ LC VCO
◆ Frequency Tuning (Varactor, SCA)
◆ Phase Noise Estimation
◆ Quadrature Phase Generator
VCO Phase Noise

\[ S_{\text{desired}} \quad S_{\text{block}} \quad \omega_{\text{RF}} \quad \Delta \omega \quad f_{\text{RF}} \quad f_{\text{IF}} \quad f_{\text{LO}} \quad \omega_{\text{IF}} \quad \omega_{\text{LO}} \quad \Delta \omega \quad \text{SNR} \quad L\{\Delta \omega\} \]
Phase Noise Requirement

\[ SNR = S_{\text{desired}} - S_{\text{noise}} = S_{\text{desired}} - [S_{\text{block}} + L\{\Delta \omega\} + 10\log(f_{ch})] \]

\[ \therefore L\{\Delta \omega\} < S_{\text{desired}} - S_{\text{block}} - SNR_{\text{min}} - 10\log(f_{ch}) \]

**Ex:** GSM

\[ S_{\text{desired}} = -102dB; \quad S_{\text{block}} = -23dB \text{ @ 600KHz} \]

\[ SNR_{\text{min}} = 9dB; \quad f_{ch} = 200KHz \]

\[ \therefore L\{\Delta \omega\} < -102 + 23 - 9 - 10\log(200K) \]

\[ <-141dBc / Hz \text{ @ 600KHz} \]
Spurious-Tone Performance

\[ S_{\text{desired}} \]

\[ S_{\text{block}} \]

\[ S_{\text{spur}} \]

\[ f_{RF} \]

\[ f_{LO} \]

\[ f_{IF} \]

\[ \omega_{RF} \]

\[ \Delta \omega \]

\[ \omega_{LO} \]

\[ \Delta \omega \]

\[ SNR \]

\[ \omega_{IF} \]

\[ \omega \]
Spurious-Tone Requirement

\[ SNR = S_{\text{desired}} - S_{\text{noise}} = S_{\text{desired}} - (S_{\text{block}} + S_{\text{spur}}) \]

\[ \therefore S_{\text{spur}} < S_{\text{desired}} - S_{\text{block}} - SNR_{\text{min}} \]

Ex: GSM

\[ S_{\text{desired}} = -102 \text{dB}; \quad S_{\text{block}} = -23 \text{dB @ 600KHz} \]

\[ SNR_{\text{min}} = 9 \text{dB}; \]

\[ \therefore S_{\text{spur}} < -102 + 23 - 9 = -88 \text{dBc} \]
Typical Figure of Merits for VCO

- Frequency: \( \sim 1 - 5 \) GHz
- Tuning Range: \( \sim 10 - 20\% \)
- Phase Noise: \(-105 \text{ dBc/Hz } @ 100 \text{ KHz}\)
- Supply Voltage: \( \sim 1.5 \text{ V} \)
- Current: \(< 10 \text{ mA}\)
Oscillation Theory

\[
\frac{Y(s)}{X(s)} = \frac{H(s)}{1 - H(s)G(s)}
\]

For steady oscillation, Barkhausen’s criteria must be simultaneously met:

\[
\left| H(s)G(s) \right| \geq 1 \\
\angle H(s) + \angle G(s) = 2n\pi
\]
Negative Resistance Model

During Oscillation:

\[ \text{Re}[Z_a(s)] + \text{Re}[Z_r(s)] = 0 \]
Negative Resistance Model

\[ A = \frac{G_m Z_{in}}{1 + G_o Z_{in}} \]

\[ Y = \frac{1}{Z_{in}} + G_o - G_m \beta = \left( \frac{1}{Z_{in}} + G_o \right) (1 - A \beta) \]

Determine the oscillation frequency

\[ \text{Im}(Y) = 0 \]
\[ \text{Im}(1 - A \beta) = 0 \]

Oscillation:

\[ A\beta > 1 \Leftrightarrow \text{Re}\left[ \left( \frac{1}{Z_{in}} + G_o \right) (1 - A \beta) \right] < 0 \]

Negative Conductance
Negative Resistance Model

\[
Z(j\omega) = \frac{1}{2\pi\sqrt{LC}}
\]

\[
f_0 = \frac{1}{2\pi\sqrt{LC}}
\]
## Ring vs LC Oscillators

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A Cascade of Delay Cells Connected in Feedback to Meet Oscillation Criteria (Barkhausen)

- Loop Gain @ $w_{osc} > 1$
- Total Phase Shift @ $w_{osc} = 2n \pi$

- For Single-Ended Design, Needs An Odd Number of Delay Cells to provide $2n \pi$ phase shift

$$f_{osc} = \frac{1}{2N\tau_d}$$
Implementation of Ring Oscillator

\[ H(j\omega_0) = \left( \frac{-GmR_0}{1 + j\omega_0R_0C_0} \right)^N \]

\[ f_{osc} = \frac{1}{2N\tau_d} \]
Delay Cells Can Simply Be Digital or Analog Inverters
Delay and Frequency Can Be Tuned By Bias Current, Device Transconductance, or Loading Resistance or Capacitance
Can Provide Rail-To-Rail Output Waveform and Wide Tuning Range
All Components Contribute Phase Noise
Delay Cells
Ring VCO – Differential Design

- Signal is Increased by 6 dB while Noise is Increased by 3 dB => Phase Noise is Improved by 3 dB
- Common-Mode Rejection (Supply, Even-Order Harmonics, Common-Mode, Substrate Noise)
- Double Power, Double Chip Area
LC VCO – Single-Ended Design

- Use Feedback Principle for Oscillation:
  - Loop Gain @ $w_{osc} > 1$
  - Total Phase Shift @ $w_{osc} = 2n \pi$
- Critical to Include Impedance Transform:
  - Not to Degrade Tank Q
  - Improve Gain for Oscillation
- Either Capacitive or Inductive Divider Can Be Used for Impedance Transformation
Feedback can be from drain to source or gate to source.
LC VCO – Single-Ended Design

\[ f_o = \frac{1}{2\pi \sqrt{(L_1 + L_2)C}} \]

\[ R_L = R_s \left( 1 + \frac{L_2}{L_1} \right)^2 \]

Hartley Oscillator
LC VCO - Single-Ended Design

Colpitts Oscillator

\[ f_o = \frac{1}{2\pi \sqrt{L \cdot \left( \frac{C_1 \cdot C_2}{C_1 + C_2} \right)}} \]

\[ R_L = R_s \left( 1 + \frac{C_2}{C_1} \right)^2 \]
- Make Use of LC Resonant Tank
- Use Negative-Gm Compensation Technique to Achieve Infinite Q for Oscillation

\[
\begin{align*}
Y_L & \quad G_P \quad -G_m \quad Y_{\text{eq}} \\
G_{\text{eq}} & = 0
\end{align*}
\]
Negative Resistance

\[\text{M}_1 \quad \text{M}_2\]

\[-G_m\]

\[I_B\]
Negative Resistance

\[ i_x = i_{d2} = -i_{d1} \]

\[ v_x = V_{gs2} - v_{gs1} \]

\[ i_x = -G_m v_x = -\frac{g_m}{2} v_x \]

At high-frequency the device capacitance and input resistance should be included in the analysis.
Differential VCO
Differential VCOs
Frequency Tuning Can Be Achieved By Tuning Capacitance Using a Varactor or a Switchable Capacitor Array (SCA)

Or Effective Inductance
PN-Junction Varactor

\[ C_T = A \frac{C_{jo}}{\sqrt{1 - \frac{V_B}{\phi_F}}} \]

\[ Q_C = \frac{1}{\omega R_s C_T} \]
PN-Junction Varactor

![Graph showing the relationship between control voltage (V) and capacitance (Y11/w pF)]

- Capacitance = \( \text{img}(Y_{11}) \cdot w \) (pF)
- Control Voltage (V) range from 0.0 to 1.8
PN-Junction Varactor

- Make Use of Depletion Capacitance of p-n Diode Junction
- n+ Contacts Are Used to Minimize Contact Resistance and thus to Maximize Q
- Reducing Size of p+ Would Minimize p+ Series Resistance

- Increasing Size of p+ Would Increase Number of Contacts and Reduce Contact Resistance
- Measurements Indicate Contact Resistance Dominates => Larger Size of p+ Diffusion is Desired for Higher Q
Accumulation-Mode Varactor

\[
\frac{1}{C_T} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}
\]

\[
Q_c = \frac{1}{\omega R_S C_T}
\]
Accumulation-Mode Varactor

![Graph showing capacitance vs. control voltage for an accumulation-mode varactor. The graph plots capacitance (in pF) on the y-axis against control voltage (V) on the x-axis, ranging from -2 to 2 V.]
Accumulation-Mode Varactor

- Similar to NMOS with N-Well Instead of P-Substrate
- $n^+$ Are Used to Minimize Parasitic p-n Junction Capacitance to Maximize Tuning
- For Gate Voltage Larger Than Flat-Band Voltage $V_{FB} \Rightarrow$ Accumulate $\Rightarrow C_T = C_{ox}$
- For Smaller Gate Voltage, Depletion Capacitance $C_{dep}$ Exists Between Oxide and N-Well $\Rightarrow 1/C_T = 1/C_{ox} + 1/C_{dep}$
- Compared to p-n Junction Capacitance, Advantages of Accumulation-Mode Capacitance Include [Soorapanth]:
  - Better Average Q
  - Larger Tuning Capacitance
Switchable-Capacitance Array

\[ \text{M}_1 \quad C_{GD} \quad R_{ON} \quad C_{GD} \quad R_{ON} \]
Larger Tuning Range

![Circuit Diagram](image)

![Graph](image)

F-VCO

F (Hz)

Vt (V)
Switchable-Capacitance Array

\[ C_{on} = C_u \]

\[ C_{off} = \frac{C_u C_{gd}}{C_u + C_{gd}} \]

\[ Q_c = \frac{1}{\omega R_{on} C_{on}} \]
Switchable-Capacitance Array

- Wide Tuning Range Can Be Achieved By Increasing Number of Bits in the Array
- Large Switch => Small Turn-On Resistance => High Q
- Large Switch => Large Parasitic Capacitance => Small Tuning Range and Limited Operating Frequency
Phase Noise Estimation

\[ L_{total}(\Delta \omega) = 10 \cdot \log \left( \frac{P_{sideband}(\omega_0 + \Delta \omega, 1Hz)}{P_{carrier}} \right) \]
Phase Noise Estimation—Leeson’s Model

\[
L(\Delta \omega) = S_{\Delta \theta}(\Delta \omega) \left[ 1 + \left( \frac{\omega_0}{2Q\Delta \omega} \right)^2 \right]
\]

\[
S_{\Delta \theta}(\Delta \omega) = \frac{\alpha}{\Delta \omega} + \frac{2FkT}{P_s}
\]
Phase Noise – Hajimiri’s Theory

\[ v(t) \]
\[ i(t) \]
\[ \tau \]

(a)

(b)
Phase Noise – Hajimiri’s Theory

\[ f(x) = \frac{1}{f_{\text{rise}}} \]

\[ \Gamma(x) = \frac{2}{f_{\text{rise}}} \]

\[ \frac{1}{f_{\text{fall}}} \]

\[ \frac{1}{f_{\text{rise}}} \]

\[ \frac{2}{f_{\text{fall}}} \]
Phase Noise – Hajimiri’s Theory

- Use Impulse Sensitivity Function (ISF) $G(x)$ which is a periodic function of phase shift for a unit impulse applied at time $t = x$
- Phase noise is maximum when noise current impulses are injected at zero-crossing point
- Phase noise is minimum when noise current impulses are injected at output peaks
Phase Noise – Hajimiri’s Theory

\[ L(\Delta \omega) = \frac{\Gamma_{\text{rms}}^2}{q_{\text{max}}^2} \cdot \frac{i_n^2 / \Delta f}{2(\Delta \omega)^2} \]

\[ L(\Delta \omega) = \frac{c_0^2}{q_{\text{max}}^2} \cdot \frac{i_n^2 / \Delta f}{8(\Delta \omega)^2} \cdot \frac{\omega_{1/f}}{\Delta \omega} \]
We see that all noise a distance $\omega$ around all the harmonics, including DC, contributes to the phase noise. DC $1/f$ noise contributes to the $1/f^3$ region.
Optimization of Phase Noise in the LC VCO

• Evaluate the optimization gate length of the active device
• Calculate minimize spectral density of each oscillator noise source by using the optimization gate length of the active device.
• Derive the impulse sensitivity function of each oscillator source after the transient simulation is done when a current noise is injected at the node of the oscillator circuit (Cadence SpectreRF).
• Combine above results to obtain for each oscillator noise source.
• Calculate Fourier Series Coefficient for each ISF
• Calculate the overall output phase noise using the results from above step.
Quadrature Phase Generator

- Divide-by-2
- Quadrature VCO
- Poly phase shifter (RC-CR network)