Layout for Analog Integrated Circuits
Outline

• What is Layout?
• Integrated Circuits Process Overview
• Design Rules for Layout
  ▪ What are they?
  ▪ Why are they important?
• Example

• Rules for Analog IC
IC -- Connecting Billions of Transistors!

- Intel Itanium Processor
- Source: ISSCC 2005
- 90nm feature size
- 7 Metal layers
- 1.7 billion transistors
City of Metals

- Millions or billions of transistors are made
- And they are connected through layers of metals
Foundries (TSMC, SMIC) need the geometrical information of these transistors and metals to make the chips. Circuit designers provide this information to foundries. They design the circuits according to the functionality and generate the layout which contains the geometrical information, for example, the size (width and length) of the transistors. Understanding layout needs an understanding of fabrication process. It is important for the circuit designers to visualize how the final chips look like for performance oriented designs.
IC Fabrication Process – Example

- Starting from Layout of a single NMOS

- Cross-section of the finished NMOS
IC Fabrication Process – a Glance (1)
IC Fabrication Process – a Glance (2)
IC Fabrication Process – a Glance (3)

- Source and Drain Diffusion
- Develop Photoresist
- Deposit Low Temperature Oxide
- Etch LTO
- Apply Photoresist
- Remove Photoresist
IC Fabrication Process – a Glance (4)
Design rules are a set of contracts between the circuit designers and process engineers.

- **Unit dimension**: Minimum line width
  - Scalable design rules: lambda parameter
  - Absolute dimensions (micron rules)
- **Intra-Layer rules**
  - Width and spacing
- **Inter-Layer rules**
  - Enclosures and overlaps
- **Special rules**
  - Antenna rules, area, density rules
Intra Layer Design Rules

- Minimum width: resolution of technology
- Maximum width
- Spacing: reliability

- **Same Potential**
  - Well
  - Active
  - Select
  - Polysilicon
  - Metal1

- **Different Potential**
  - Contact or Via Hole
Inter Layer Design Rules (1)

- Overlap
- Ex: Gate overlap with active region

A 3-D perspective
Inter Layer Design Rules (2)

• Enclosure
• Ex: Vias and Contacts
Layout Design Rules Example – An Inverter

(a) Layout

(b) Cross-Section along A-A’
Analog IC Layout

• One of the most important features analog design depends on – matching
• Matching means two are ‘identical’ (hopefully)!

Analog Circuits use matched transistors! Where?

• Differential pairs want **voltage** matching on $V_{GS}$
• Current mirrors want **current** matching
• etc.
Real Transistors

What we draw and hope

Real transistor

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Geometric Effects on Matching

- **Increased Gate Area** minimizes impact of local fluctuations
  
  Large transistors match more precisely.

- **Longer channels** reduce linewidth variations and channel length modulation
  
  Long-channel transistors match more precisely.

- Orientation of MOSFET matters.

  Gate Area, Oxide thickness, Channel length modulation, Orientation, …
Gate Area

$V_{t\text{ mismatch}}$: $S_{V_t} = \text{standard deviation}$

$$S_{V_t} = C_{V_t} / (W_{\text{eff}} L_{\text{eff}})^{1/2}$$

Where $C_{V_t} = \text{constant}$.

- Only applies to carefully laid out MOS for optimal matching.
- $L_{\text{eff}}, W_{\text{eff}} \Rightarrow L_d, W_d$ if they are several times greater than minimum.
Orientation

Several % mismatch error:
- Si wafer is under stress due to processing.
- The stress produces anisotropic effect on the carrier mobility, etc.
- Different orientation ➔ different stress effect on the transconductance

- Stress-induced mobility variation ➔ several %
- For example, tilted wafer ➔ as much as 5% in matching errors.
Orientation

Layout Editing:

- Be careful with Cell editing *when the matched transistors belong in different cells!*
- **Group matched devices into the same cell**
- May be more difficult to understand in the Schematics
- But safer for the matching!
Orientation

*Mirror-image* layout vs. *Superimposable* layout:

- Mask misalignment $\Rightarrow$ same effect on superimposable; but opposite effect on mirror-image.
- So, be careful on asymmetric devices such as Extended Drain MOS.
Example of Orientation-Dependent Mismatch:

**TILTED IMPLANTS**
Example of Orientation-Dependent Mismatch:

**TILTED IMPLANTS**

Consider matching two transistors: $A$ and $B$

$D_A S A_B D_B$
Poly gate is one of the most important structure

**Diffusion and Etch effects on Matching**

**Effects of Poly Gate etching**

- Consider the mask-step of defining Poly Gates:
  - Deposit Poly → cover with oxide → Mask pattern for opening → remove Poly open region by etching

- Etch rate depends on the size of Opening:
  - Larger opening → faster etch.
Diffusion and Etch effects on Matching

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(2) Diffusion and Etch effects on Matching

- Dummy Gates need be electrically connected to prevent spurious signal.
- Best to connect Dummy Gates to the Backgate.
(3) Contacts over the Gate Poly

- Contacts in the active Gate region $\Rightarrow$ gross variations in $V_t$
- Gate contacts must be **outside the active region**, on thick field-oxide.
- Probably because of grain size, work function, dopants, stress, …
(3) Contacts over the Gate Poly

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(4) Diffusions near the Channel

Deep Diffusions (e.g., deep-N+ sinker, Nwell, …) ➔
diffusion tails extend much farther than the junctions.
Spacing BETWEEN Matched Channels AND Deep diffusion boundaries ➔ must be 2 times the Junction Depth!

• Spacing BETWEEN Active Gate regions (of matched transistor) AND the edge of the nearest NBL region ➔ at least 150% of the epi thickness.
Common-Centroid Layout of MOS Transistors

- Consider a MOS transistor with a couple of Gate fingers.
- Then consider matching two such transistors.

![Diagram of MOS transistors A and B with common centroid layout]
Common-Centroid Layout of MOS Transistors

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The MOS pair = A B B A
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Use $S$, $D$ as subscripts $\rightarrow dA_s B_d B_s A_d$

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Rules of Common-Centroid Layout

1. **Coincidence**: The centroids of the matched devices must at least approximately coincide.

2. **Symmetry**: The array should be symmetric wrt both X- and Y-axes.

3. **Dispersion**: The segments of each device should be distributed throughout the array as uniformly as possible.

4. **Compactness**: The array should be as compact as possible. Ideally, nearly square.

5. **Orientation**: Matched device should possess equal Chirality.
Simple Interdigation Patterns for MOS Transistor:

1. \((S_{AD}A)(S_{DB}B_{S}B_{D}B)(S_{AD}A)_{S}\) \(A:B = 1:1\)

2. \((D_{AS}B_{D}-D_{BS}A_{D})-(D_{AS}B_{D}-D_{BS}A_{D})\)

3. \((D_{AS}B_{D}B_{S}A)_{D}\)

4. \((S_{AD}A_{S}B_{D}B)_{S}(B_{D}B_{S}A_{D}A_{S})\)

5. \((S_{AD}A_{S}B_{D}B_{S}A_{D}A)_{S}\) \(A:B = 2:1\)

6. \((S_{AD}A_{S}B_{D}-S_{AD}A_{S}-D_{BS}A_{D}A)_{S}\) \(A:B = 3:1\)

7. \((S_{AD}A_{S}B_{D}B_{S}C_{D}C)_{S}(C_{D}C_{S}B_{D}B_{S}A_{D}A_{S})\) \(A:B:C = 1:1:1\)
Bandgap Transistors

• 1:8 matching is normally chosen for matching.
MOS Transistor Matching

*MOS transistors can be optimized either for voltage matching or for current matching, but not for both!*

==> Why?
Suppose two transistors, M1 and M2, operate at equal drain currents. Then, the possible voltage mismatch:

OFFSET Voltage: \[ \Delta V_{GS} = \Delta V_t - V_{ov} \left( \frac{\Delta k}{2k_2} \right) \]

- To minimize \( \Delta V_{GS} \):
- use large \( W/L \) and low operating currents.
- minimize \( V_{ov} \): \( V_{ov} = 0.1 \text{ volts or less} \).
Current matching

The mismatch between $I_{D1}$ and $I_{D2}$:

$$\frac{I_{D2}}{I_{D1}} = \frac{k_2}{k_1} \left( 1 + 2\frac{\Delta V_t}{V_{ov}} \right)$$

$$\frac{\Delta I_d}{I_d} = \frac{\Delta k}{k} + 2\frac{\Delta V_t}{V_{ov}}$$

To optimize:

- use reasonably large $V_{ov}$: $V_{ov} = 0.3 \text{ V or more}$!

So, $V_{ov} = 0.1 \text{ V or less for voltage}$ matching and $V_{ov} = 0.3 \text{ V or more for current}$ matching.

Next is the effect of geometric factors on the matching!
Summary

• Layout is the output that the circuit designers deliver to the process engineers for fabrication.

• Design rules are a set of contracts between the circuit designers and process engineers.

• It is important to understand the design rules for quality design of circuits:
  ▪ High speed, low power, yield, etc.

• Matching is one important property analog circuits rely on:
  ▪ Good matching requires good layout practice.