1. Introduction

If the automobile had followed the same development cycle as the computer, a Rolls-Royce would today cost $100, get one million miles to the gallon and explode once a year.
outline

- Course Introduction
- a brief history
- Design Metrics
- DIC characteristics
- Design partitioning/CMOS logic
- Semiconductor processing
Semiconductor processing

- Semiconductor fabrication
- Layout fundamental
- **Semiconductor testing**
- Semiconductor assembling
Different Electrical Tests for IC Production (From Design Stage to Packaged IC)

<table>
<thead>
<tr>
<th>Test</th>
<th>Stage of IC Manufacture</th>
<th>Wafer- or Chip-Level</th>
<th>Test Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC Design Verification</td>
<td>Pre-Production</td>
<td>Wafer level</td>
<td>Characterize, debug and verify new chip design to insure it meets specifications.</td>
</tr>
<tr>
<td>In-Line Parametric Test</td>
<td>Wafer fabrication</td>
<td>Wafer level</td>
<td>Production process verification test performed early in the fabrication cycle (near front-end of line) to monitor process.</td>
</tr>
<tr>
<td>Wafer Sort (Probe)</td>
<td>Wafer fabrication</td>
<td>Wafer level</td>
<td>Product functional test to verify each die meets product specifications.</td>
</tr>
<tr>
<td>Burn-In Reliability</td>
<td>Packaged IC</td>
<td>Packaged chip level</td>
<td>ICs powered up and tested at elevated temperature to stress product to detect early failures (in some cases, reliability testing is also done at the wafer level during in-line parametric testing).</td>
</tr>
<tr>
<td>Final Test</td>
<td>Packaged IC</td>
<td>Packaged chip level</td>
<td>Product functionality test using product specifications.</td>
</tr>
</tbody>
</table>
Automated Electrical Tester
Wafer Fab Process Flow with Test

Wafer start → Unpatterned wafer → Diffusion → Implant → Photo → Etch → Polish → Thin Films → Test/Sort → Completed wafer
**Wafer Test**

- In-line Parametric Test (a.k.a. wafer electrical test, WET)
  - In-line test structure
  - In-line test type
  - In-line test data explain
  - In-line test equipment
In-line Parametric Test Systems

- Probe card interface
- Wafer positioning
- Tester instrumentation
- Computer as host or server/network
Probe Card for Automatic Tester
## Examples of Test Structure

<table>
<thead>
<tr>
<th>Test Structure</th>
<th>Fault Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Discrete transistors</td>
<td>Leakage current, breakdown voltage, threshold voltage and effective channel length</td>
</tr>
<tr>
<td>Various line widths</td>
<td>Critical dimensions</td>
</tr>
<tr>
<td>Box in a box</td>
<td>Critical dimensions and overlay registration</td>
</tr>
<tr>
<td>Serpentine structure over oxide steps</td>
<td>Continuity and bridging</td>
</tr>
<tr>
<td>Resistivity structure</td>
<td>Film thickness</td>
</tr>
<tr>
<td>Capacitor array structure</td>
<td>Insulator materials and oxide integrity</td>
</tr>
<tr>
<td>Contact or via string</td>
<td>Contact resistance and connections</td>
</tr>
</tbody>
</table>
Data Trends

- The same die location keeps failing a parameter on a wafer.
- The same parameter is consistently failing on different wafers.
- There is excessive variation (e.g., > 10%) in measurement data from wafer to wafer.
- Lot-to-lot failure for the same parameter, indicating a major process problem.
Wafer Sort

- Wafer Sort (a.k.a. wafer probe)
  - DC testing
  - Output checking
  - Function testing
- The Objectives of Wafer Sort
  - Chip functionality: verify the operation of all chip functions to insure only good chips are sent to the next IC manufacturing stage of assembly and packaging.
  - Chip sorting: sort good chips based on their operating speed performance (this is done by testing at several voltages and varying timing conditions).
  - Fab yield response: Provide important fab yield information to assess and improve the performance of the overall fabrication process.
  - Test coverage: Achieve high test coverage of the internal device nodes at the lowest cost.
Wafer Bin Map with Bin Failures

Device: Example
Lot: Example
Wafer: 200 mm
Layer: Hardware Bins
Yield: 79.54%
Good: 70
Total: 88

Good
Bad
Reduced Partial Die on Large Wafer

200 mm

14.5% partial die

10.8% partial die

300 mm
Reduced Time to Product Maturity for DRAM Production

![Graph showing reduced time to product maturity for DRAM production.](image-url)
Semiconductor processing

- Semiconductor fabrication
- Layout fundamental
- Semiconductor testing
- **Semiconductor assembling**
Packaging Requirements

- Electrical: Low parasitics
- Mechanical: Reliable and robust
- Thermal: Efficient heat removal
- Economical: Cheap
Important Functions of IC Packaging

- Protection from the environment and handling damage.
- Interconnections for signals into and out of the chip.
- Physical support of the chip.
- Heat dissipation.
Typical IC Packages

Dual in-line package (DIP)

Single in-line package (SIP)

Thin small outline package (TSOP)

Quad flat pack (QFP)

Plastic leaded chip carrier (PLCC)

Leadless chip carrier (LCC)
## Levels of IC Packaging

<table>
<thead>
<tr>
<th>First level packaging: IC packaging</th>
<th>Metal leads for mounting onto printed circuit board</th>
</tr>
</thead>
<tbody>
<tr>
<td>2nd level packaging: Printed circuit board assembly</td>
<td>Surface-mount chips are soldered on top of tinned pads on the PCB.</td>
</tr>
<tr>
<td>Final product assembly: Final assembly of circuit boards into system</td>
<td>PCB subassembly</td>
</tr>
</tbody>
</table>

- **Leads**: Pins are inserted into holes then soldered on rear of PCB.
- **Pins**: Edge connector plugs into main system.
- **Surface-mount chips**: Are soldered on top of tinned pads on the PCB.
- **PCB subassembly**: Main electronics assembly board.
Traditional Assembly

- Wafer preparation (backgrind)
- Die separation
- Die attach
- Wire bonding
Schematic of the Backgrind Process

- Downforce
- Rotating and oscillating spindle
- Wafer on rotating chuck
- Table rotates only during indexing of wafers
Wafer Saw and Sliced Wafer
Typical Leadframe for Die Attach
Epoxy Die Attach

Die

Epoxy

Leadframe
Wires Bonded from Chip Bonding Pads to Leadframe

- Die
- Bond wire
- Bonding pad
- Moulding compound
- Leadframe
- Pin tip
Wirebonding Chip to Leadframe
Traditional Packaging

- Plastic Packaging
- Ceramic Packaging
- TO-Style Metal Package(old)
General package mode

Plastic Dual In-Line Package (DIP) for Pin-In-Hole (PIH) 1970s-1980s

Single In-Line Package (SIP), decreasing capacity and cost for Memory application

Thin Small Outline Package (TSOP) for Memory and smartcard

Single In-Line Memory Module (SIMM)
General package mode

Quad Flatpack (QFP) with Gull Wing Surface Mount Leads

Plastic Leaded Chip Carrier (PLCC) with J-Leads for Surface Mount

Leadless Chip Carrier (LCC)

Laminated Refractory Ceramic Process Sequence
Ceramic interconnect layers

4-layer laminate
Advanced Packaging

- Flip chip
- Ball grid array (BGA)
- Chip on board (COB)
- Tape automated bonding (TAB)
- Multichip modules (MCM)
- Chip scale packaging (CSP)
- Wafer-level packaging
Advanced Packaging

Flip Chip Package

Connecting pin
Substrate
Metal interconnection
Via
Silicon chip
Solder bump on bonding pad

Flip Chip Area Array Solder Bumps Versus Wirebond

Flip chip bump area array

Solder bump
Chip
Epoxy
Substrate
Ball Grid Array

- Molded cover
- Wire
- Substrate
- Metal via
- Solder ball
- Bonding pad
- Chip
- Epoxy
- Thermal via
Multichip Module (MCM)
Summary

- MOS Transistors are stack of gate, oxide, silicon
  Can be viewed as electrically controlled switches
- Build logic gates out of switches
- Draw masks to specify layout of transistors
- Using different packaging & assembling tech.
- to start designing schematics and layout for a simple chip!