Ratioed Logic
Ratioed Logic design

- Basic concept
- Resistive load
- Depletion NMOS
- Pseudo NMOS
- DCVSL logic
- Pseudo NMOS logic effort
Ratioed Logic

Goal: to reduce the number of devices over complementary CMOS
How to obtain a good load

- What is a good load
  - Low power
  - $V_{OL}$ tend to zero
  - Charge time short (large charge current)
- Memory address decoder match the structure
  - Low power when address hold the line
  - Change quickly when address content is changed
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Ratioed Logic-resistive load

- Resistive Load
- \( V_{DD} \)
- \( R_L \)
- \( F \)
- \( V_{SS} \)

- \( V_{OH} = V_{DD} \)
- \( V_{OL} = \frac{R_{PN}}{R_{PN} + R_L} \)
- Assymmetrical response
- Static power consumption
- \( t_{pL} = 0.69 R_L C_L \)

N transistors + Load
Resistive load

- Could not be to low
  \[ V_{OL} = \frac{R_{PDN}}{R_{PDN} + R_L} V_{DD} \]
  - In order to obtain wide range low noise margin, \( R_L \gg R_{PDN} \)
  - Then resistive size should be adjust

- Could not be to high
  - Then enough large current could give quick switch time, because
    \[ t_{pLH} = 0.69 R_L C_L \]
    \[ t_{pHL} = 0.69 (R_L \parallel R_{PDN}) C_L \]
  - Decrease power consumption as soon as possible
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Active Loads

Depletion Load

$V_{DD}$

$V_T < 0$

PDN

$V_{SS}$

In

In

In

PMOS Load

$V_{DD}$

$V_{SS}$

PDN

$V_{SS}$

In

In

In

Depletion load NMOS

pseudo-NMOS

Depletion load has negative threshold voltage
Depletion NMOS load

- It is reasonable when we assume the load transistor works at saturate state, just like a current source
  
  \[ I_L = \frac{k_{n,\text{load}}}{2} |V_{Tn}|^2 \]

- Practically, the load curve slant down
  - Load transistor’s source is connect with output, which \( V_{SB} \) will effect threshold voltage of the transistor
  - Compared with resistive load, depletion load has smaller area
    - 40k\( \Omega \) resistive load need 3200\( \mu \)m2(0.5\( \mu \)m) which could occupy 1000 unit transistor
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Pseudo-NMOS ratios computing

• PMOS’s source and substrate voltage is always zero, that means no body effect
• Load transistor’s saturate current is

\[ I_L = \frac{k_p}{2} (V_{DD} - |V_{Tp}|)^2 \]

\textit{pMOS load current is larger than that of nMOS}
Pseudo NMOS logic design rule

- Static power
  \[ P_{\text{average}} = V_{dd}I_{\text{low}} = \frac{k_p}{2} V_{dd} (V_{dd} - V_T)^2 \]

- Constrains should be regarded
  - \(I_L\) should be low in order to decrease power
  - \(V_{OL} = I_L R_{PDN}\) should be lower in order to obtain effective low voltage
  - \(I_L\) should high in order to decrease \(t_{pLH} = (C_L V_{dd})/(2I_L)\)
  - \(R_{PDN}\) should be small in order to decrease \(t_{pHL} = 0.69R_{PDN}C_L\)

**Pull-down transistors should be wider, but we can not benefit from both power and delay**
Pseudo-NMOS VTC

\[ V_{in} \quad [V] \]

\[ V_{out} \quad [V] \]

- \( W/L_p = 4 \)
- \( W/L_p = 2 \)
- \( W/L_p = 0.5 \)
- \( W/L_p = 0.25 \)

Digital IC
Load curve analysis

- Resistive load
  \[ I_L = \frac{V_{DD} - V_{out}}{R_L} \]
  - More output voltage, lower charge current, which increase charge time
- Ideally, constant current source
  - Charge current does not be decreased by output voltage
Pseudo-NMOS NMOS ratioed logic

- Pseudo-NMOS ratioed logic merits
  - N-fan-in needs N+1 transistors, with smaller area and parasitic capacity
  - Every input only connects with one transistor, which load capacity is smaller as front stage logic.

- Shortcoming
  - Static power, 1mW per logic, 50W consumption if chip has 100,000 such logic structure!

- Application
  - Can not fit for large scale circuit
  - Only apply on high speed circuit
  - Only apply on 1-state on most output (such as address decoder)
  - Large fan-in
Improved Loads

Adaptive Load
Improved Loads (2)

\[ V_{DD} \quad V_{DD} \]

\[ M1 \quad M2 \]

\[ Out \quad Out \]

\[ A \quad PDN1 \quad A \quad PDN2 \]

\[ A \quad B \quad B \]

\[ V_{SS} \quad V_{SS} \]

Differential Cascode Voltage Switch Logic (DCVSL)
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DCVSL Example

XOR-NXOR gate

Out

Voltage [V]

Time [ns]

0.2 0.4 0.6 0.8 1.0

-0.5 0 0.5 1.5 2.5
Pseudo-nMOS Power

- Pseudo-nMOS draws power whenever $Y = 0$
  - Called static power $P = I \cdot V_{DD}$
  - A few mA / gate * 1M gates would be a problem
  - This is why nMOS went extinct!
- Use pseudo-nMOS sparingly for wide NORs
- Turn off pMOS when not in use

![Diagram of Pseudo-nMOS circuit]
Pass-Transistor Logic
Pass- transistor logic outline

- **Pass-transistor principle**
- Pass-transistor VTC
- How to solve pass-transistor threshold drop issue
  - Solution 1: Level Restoring Transistor Resistive issue
  - Solution 2: Single Transistor Pass Gate with VT=0
  - Solution 3: Transmission Gate Complementary Pass-Transistor Logic
- Transmission gate principle
- Some issues of transmission gate
  - Resistive issue
  - Delay issue
Pass-Transistor Logic

- N transistors
- No static consumption

Pass-transistor logic is a path, not a road connected with rail directly!
Example: AND Gate

\[ F = AB \]
NMOS-Only Logic

- NMOS keep “on”, then $V_{GS} > V_t$
- $V_{DG} = 0$, which means NMOS always works in the saturation state
NMOS-only Switch

\[ C = 2.5\text{V} \quad C = 2.5\text{V} \]

\[ A = 2.5\text{V} \quad A = 2.5\text{V} \]

\[ B \quad B \quad B \]

\[ M_2 \quad M_n \quad M_1 \]

\[ V_B \text{ does not pull up to 2.5V, but } 2.5\text{V} - V_{TN} \]

Threshold voltage loss causes static power consumption

*NMOS has higher threshold than PMOS (body effect)*
The proper way of cascading pass gates

- Weak for passing high voltage
  
  \[ V_s = \min\{V_G - V_T, V_D\} \]

- Proper way of cascading pass transistors, which will not accumulate threshold drop
Output of passing-transistor should not be connected with the gate of next stage
Nonrestoring Tristate

- Transmission gate acts as tristate buffer
  - Only two transistors
  - But *nonrestoring*
    - Noise on A is passed on to Y
Tristate Inverter

- Tristate inverter produces restored output
  - Violates conduction complement rule
  - Because we want a Z output
Tristate Inverter

- Tristate inverter produces restored output
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```
A
EN
Y
EN

A
Y
EN = 0
Y = 'Z'

A
Y
EN = 1
Y = \bar{A}
```
Gate-Level Mux Design

- \( Y = SD_1 + \overline{SD}_0 \) (too many transistors)
- How many transistors are needed?
Gate-Level Mux Design

- \( Y = SD_1 + \bar{S}D_0 \) (too many transistors)
- How many transistors are needed? 20
Transmission Gate Mux

- Nonrestoring mux uses two transmission gates
Transmission Gate Mux

- Nonrestoring mux uses two transmission gates
  - Only 4 transistors
Inverting Mux

- Inverting multiplexer
  - Use compound AOI22
  - Or pair of tristate inverters
  - Essentially the same thing
- Noninverting multiplexer adds an inverter
4:1 Multiplexer

- 4:1 mux chooses one of 4 inputs using two selects
  - Two levels of 2:1 muxes
  - Or four tristates
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Complementary Pass Transistor Logic

(a)

(b)

AND/NAND

OR/NOR

EXOR/NEXOR
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Solution 1: Level Restoring Transistor

- Advantage: Full Swing
- Restorer adds capacitance, takes away pull down current at X
- Ratio problem
Restorer Sizing

- Upper limit on restorer size
- Pass-transistor pull-down can have several transistors in stack

\[
\begin{align*}
\frac{W}{L} &= 1.0/0.25 \\
\frac{W}{L} &= 1.25/0.25 \\
\frac{W}{L} &= 1.50/0.25 \\
\frac{W}{L} &= 1.75/0.25
\end{align*}
\]

Voltage [V]

Time [ps]

0 100 200 300 400 500
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Solution 2: Single Transistor Pass Gate with $V_T=0$

$V_{DD}$

0V 2.5V $V_{DD}$

$V_{DD}$ 0V $Out$

2.5V

WATCH OUT FOR LEAKAGE CURRENTS
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  • Transmission gate principle
  • Some issues of transmission gate
    • Resistive issue
    • Delay issue
Solution 3: Transmission Gate

\[ C = 2.5 \text{ V} \]
\[ A = 2.5 \text{ V} \]
\[ C = 0 \text{ V} \]
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Pass-Transistor Based Multiplexer

Diagram showing the Pass-Transistor Based Multiplexer with labels for A, B, VDD, GND, I, S, and n1, n2.
Transmission Gate XOR
Transmission Gate Full Adder

Similar delays for sum and carry
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More detail about a processing of low-to-high

- Two transistors stories
  - NMOS
    - For $V_{GS}=V_{DS}$, $V_{GD}=0<V_t$, then NMOS always works in the saturation or off state
  - PMOS
    - For $V_{GS}=-2.5V$, transistor turn from saturation to linear state
  - More detail

\[
\begin{align*}
V_{out} < |V_{tp}| &: \text{NMOS and PMOS are in saturation} \\
|V_{tp}| < V_{out} < V_{dd} - V_{tn} &: \text{NMOS in satur., PMOS in linear} \\
V_{dd} - V_{tn} < V_{out} &: \text{NMOS cut off, PMOS in linear}
\end{align*}
\]
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• Transmission gate principle
• **Some issues of transmission gate**
  • Resistive issue
  • **Delay issue**
• Complementary Pass-Transistor Logic
Delay in Transmission Gate Networks

- Many applications use transmission like that
- Replaced by their equivalent resistances
Computing delay time

- How to do
  - Solving the differential equation

\[
\frac{\partial V_i}{\partial t} = \frac{1}{R_{eq} C} \left( V_{i+1} - V_i - (V_i - V_{i-1}) \right)
\]

\[
\frac{\partial V_i}{\partial t} = \frac{1}{C} (I_{i+1} - I_i)
\]

- It is too complex to find precise solution, we have to find some approximate solution
A close solution

- Delay time is

\[
\tau (V_n) = \sum_{k=0}^{n} CR_{eq} k = CR_{eq} \frac{n(n + 1)}{2}
\]

- Break chain and Insert buffer
Transmission gate delay optimization

- Total delay time
  - Assume all has \( n \) transmission gate, break chain every \( m \) switches, buffer delay time is \( t_{buf} \)

\[
\begin{align*}
  t_p &= 0.69 \left[ \frac{n}{m} CR_{eq} \frac{m(m+1)}{2} \right] + \left( \frac{n}{m} - 1 \right) t_{buf} \\
  &= 0.69 CR_{eq} \frac{n(m + 1)}{2} + \left( \frac{n}{m} - 1 \right) t_{buf}
\end{align*}
\]
Optimal number of switch

\[ m_{optimal} \]

\[
\frac{\partial t_p}{\partial m} = 0
\]

\[
\frac{\partial t_p}{\partial m} = 0.69CR_{eq} \frac{n}{2} - \frac{nt_{buf}}{m^2} = 0
\]

\[
m_{optimal} = 1.7 \sqrt{\frac{t_{buf}}{CR_{eq}}} = 1.7 \alpha
\]

It is independent with n